

THIN FILM TRANSISTOR AND METHOD OF MANUFACTURING THE SAME

BACKGROUND OF THE INVENTION

Field of the invention

The present invention relates to a thin film transistor and a method of manufacturing the same, and, more particularly, to a thin film transistor manufactured according to a method that provides high electrified mobility, high reliability and simplified manufacturing.

Description of Related Art

A poly silicon layer is generally used as a semiconductor layer of a thin film transistor (TFT). The poly silicon layer is formed such that an amorphous silicon layer is first deposited on a substrate and crystallized at a predetermined temperature. A method of crystallizing the amorphous silicon layer includes an excimer laser annealing (ELA) technique, a solid phase crystallization (SPC) technique, and a metal induced lateral crystallization (MILC) technique.

Of these techniques, the MILC technique is disclosed in U.S. Pat No. 6,097,037 and has an advantage in that the amorphous silicon layer is crystallized at a relatively low temperature and at a relatively short processing time in comparison with the ELA technique and the SPC technique.

FIGs. 1A to 1B are cross-sectional views illustrating a process of manufacturing the TFT using the MILC technique according to conventional methods.

Referring to FIG. 1A, an amorphous silicon layer 11 is formed such that an amorphous silicon is deposited on an insulating substrate 10 using a low pressure chemical vapor deposition (LPCVD) technique and patterned in the form of an island.

A gate insulating layer 12 and a gate electrode 13 are sequentially formed on the amorphous silicon layer 11 while exposing both end portions of the amorphous silicon layer 11.

A high-density impurity is ion-implanted into the exposed end portions of the amorphous silicon layer 11 to form source and drain regions 11S and 11D. A non-doped portion of the amorphous silicon layer 11 acts as a channel area 11C.

5 A photoresist pattern 15 is formed on the amorphous silicon layer 11 and covers the gate insulating layer 12 and the gate electrode 13. At this juncture, both end portions of the amorphous silicon layer 11 are not covered with the photoresist pattern 15. Thereafter, a metal layer 14 is deposited over the entire surface of the insulating substrate 10 using a sputtering technique. Preferably, the metal layer 14 is made of Ni, Pd, Ti, Ag, Au, Al, or Sb.

10 Referring now to FIG. 1B, the photoresist pattern 15 is removed using a lift-off technique, whereupon offset regions 17 are formed. Subsequently, the amorphous silicon layer 11 is crystallized by a furnace to form a poly silicon layer 11a. At this juncture, a portion of the amorphous silicon layer 11 that directly contacts the metal layer 14 is crystallized by a metal induced crystallization (MIC) technique, and the offset regions 17 and the channel area 11C are crystallized by the MILC technique.

15 In the conventional method of manufacturing the TFT using the MILC technique, traps are prevented since the boundaries between the MIC and MILC regions are located outside the channel area 11C, *for example*, within the source and drain regions 11S and 11D.

20 However, the conventional method of manufacturing the TFT using the MILC technique additionally requires a mask process to form the offset regions 17, thereby lowering productivity and increasing the production costs.

Also, since a crystallization is performed using the MILC technique after the gate insulating layer 12 and the gate electrode 13 are formed on the amorphous silicon layer 11, an

interface characteristic between the gate insulating layer 12 and the channel area 11C deteriorates, and many trap sites are provided, whereby the electric field mobility is lowered.

In addition, an MILC front 11F, including a metal silicide, exists in the channel area 11C and serves as a defect of the TFT, thereby deteriorating reliability of the TFT. Here, the MILC front 11F is referred to as that portion where lateral growths meet each other when the amorphous silicon layer 11 is crystallized by the MILC technique. Such an MILC front 11F contains more metal components than other portions and becomes a defect of the semiconductor layer.

In order to locate the MILC front 11F outside the channel area 11C, a method is introduced such that the MIC region is non-symmetrically formed centering on the channel area 11C to perform a crystallization. That method is disclosed in IEEE Electron Device Letters, vol. 21, no. 7, July 2000, and is entitled "The Effects of Electrical Stress and Temperature on the Properties of Polycrystalline Silicon Thin Film Transistor Fabricated by Metal Induced Lateral Crystallization." However, this method has a problem in that a crystallization is non-symmetrically performed and thus a processing time for crystallization is increased.

SUMMARY OF THE INVENTION

To overcome the problems described above, preferred embodiments of the present invention provide a thin film transistor (TFT) having a high electric field mobility.

It is another object of the present invention to provide a TFT having a high productivity.

It is still another object of the present invention to provide a TFT having a high reliability.

In order to achieve the above objects, the preferred embodiments of the present invention provide a method of manufacturing a thin film transistor, comprising: a) forming an amorphous

silicon layer and a blocking layer on an insulating substrate; b) forming a photoresist layer having first and second photoresist patterns on the blocking layer, the first and second photoresist patterns spaced apart from each other; c) etching the blocking layer using the first photoresist pattern as a mask to form first and second blocking patterns; d) reflowing the photoresist layer, so that the first and second photoresist patterns abut on each other so as to entirely cover the first and second blocking patterns; e) forming a metal layer over the entire surface of the insulating substrate; f) removing the photoresist layer to expose the blocking layer and an offset region between the blocking layer and the metal layer; g) crystallizing the amorphous silicon layer to form a poly silicon layer, wherein a portion of the amorphous silicon layer directly contacting the metal layer is crystallized through a metal induced crystallization (MIC), and the remaining portion of the amorphous silicon layer is crystallized through a metal induced lateral crystallization (MILC), so that an MILC front exists on a portion of the poly silicon layer between the first and second blocking patterns; h) etching the poly silicon layer using the first and second blocking patterns as a mask to form first and second semiconductor layers and to remove the MILC front; and i) removing the first and second blocking patterns.

The present invention further provides a method of manufacturing a thin film transistor, comprising: a) forming an amorphous silicon layer on an insulating substrate; b) forming a first photoresist layer on the amorphous silicon layer while exposing edge portions of the amorphous silicon layer; c) forming a metal layer over the entire surface of the insulating substrate; d) removing the first photoresist layer to expose a portion of the amorphous silicon layer under the first photoresist layer; e) crystallizing the amorphous silicon layer to form a poly silicon layer, wherein a portion of the amorphous silicon layer directly contacting the metal layer is crystallized through a metal induced crystallization (MIC), and the remaining portion of the

amorphous silicon layer is crystallized through a metal induced lateral crystallization (MILC), so that an MILC front exists on an MILC portion of the poly silicon layer crystallized by the MILC; f) removing the metal layer; g) providing a second photoresist layer having first and second photoresist patterns on the MILC of the poly silicon layer to expose the MILC front, the first and
5 second photoresist patterns spaced apart from each other; h) etching the poly silicon layer using the first and second photoresist patterns as a mask to form first and second semiconductor layers and to remove the MILC front; and i) removing the first and second photoresist patterns.

The metal layer is preferably made of Ni or Pd and preferably has a thickness of hundreds of Å. Preferably, a crystallization of the amorphous silicon layer is performed at a temperature
10 of 400 °C to 600 °C. The method further includes, after the step (i), surface-treating the first and second semiconductor layers. The surface treatment is preferably performed using a dry-etching technique or an HF etching solution of 0.1 % to 20 %. The blocking layer is patterned using a dry-etching technique or an HF etching solution of 0.1 % to 20 %. The method further includes, before the step (a), forming a buffer layer on the insulating substrate. The buffer layer, the
15 amorphous silicon layer, and the blocking layer are sequentially formed through a plasma-enhanced chemical vapor deposition (PECVD) technique or the buffer layer is formed before the amorphous silicon layer and the blocking layer are sequentially formed through the PECVD technique.

The method further includes, after the step (i): j) forming a gate insulating layer over the
20 entire surface of the insulating substrate; k) forming a gate electrode on the gate insulating layer over the first and second semiconductor layers; l) forming first source and drain regions and second source and drain regions in the first and second semiconductor layers, respectively; m) forming an interlayer insulating layer over the entire surface of the insulating substrate; n)

etching the interlayer insulating layer to form first source and drain contact holes and second source and drain contact holes; the first source and drain contact holes exposing the first and second source and drain regions, the second source and drain contact holes exposing the second and second source and drain regions, respectively; and o) forming source and drain electrodes, the source electrodes electrically connected to the first and second source regions through the first and second source contact holes, the drain electrodes electrically connected to the first and second drain regions through the first and second drain contact holes.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which like reference numerals denote like parts, and in which:

FIGs. 1A to 1B are cross-sectional views illustrating a process of manufacturing the thin film transistor (TFT) using an MILC technique according to conventional methods;

FIGs. 2A to 2I are plan views illustrating a process of manufacturing a TFT according to an embodiment of the present invention;

FIGs. 3A to 3I are cross-sectional views taken along line III-III of FIG. 2I, illustrating a process of manufacturing the TFT according to an embodiment of the present invention;

FIGs. 4A to 4G are plan views illustrating a TFT according to another embodiment of the present invention; and

FIGs. 5A to 5G are cross-sectional views taken along line V-V of FIG. 4G.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Reference will now be made in detail to preferred embodiments of the present invention, an example of which is illustrated in the accompanying drawings.

Referring to FIGs. 2A and 3A, a buffer layer 21, an amorphous silicon layer 22 and a blocking layer 23 are sequentially formed on an insulating substrate 20. The buffer layer 21 is preferably made of an oxide layer and serves to prevent an impurity from being diffused into a semiconductor layer which will be formed in a subsequent process. The blocking layer 23 is
5 preferably made of an oxide layer.

There are two methods to form the buffer layer 21, the amorphous silicon layer 22, and the blocking layer 23. A first method is that after the buffer layer 21 is formed on the insulating substrate 20, the amorphous silicon layer 22 and the blocking layer 23 are deposited using a plasma-enhanced chemical vapor deposition (PECVD) technique. The second method is that the
10 buffer 21, the amorphous silicon layer 22, and the blocking layer 23 can be sequentially deposited using the PECVD technique.

A photoresist pattern 24 is formed on the blocking layer 23. The photoresist pattern 24 has the same pattern as a mask to form a dual-channel semiconductor layer which will be formed in a subsequent process. In other words, the photoresist pattern 24 includes first and second
15 photoresist patterns 24-1 and 24-2, which are spaced apart from each other as shown in FIG. 2A.

Referring now to FIGs. 2B and 3B, using the photoresist pattern 24 as a mask, the blocking layer 23 is patterned using a dry-etching technique or an HF etching solution while exposing both end portions of the amorphous silicon layer 22, so that the blocking layer 23 includes first and second blocking patterns 23-1 and 23-2. The first and second blocking patterns
20 23-1 and 23-2 are spaced apart from each other.

In FIGs. 2A to 2I and 3A to 3I, reference numerals in parentheses denote parts which are not shown due to a viewing angle.

Referring now to FIGs. 2C and 3C, the photoresist pattern 24 is reflowed to entirely cover the patterned blocking layer 23. A first reflowed photoresist pattern 24-1a and a second reflowed photoresist pattern 24-2a of the reflowed photoresist pattern 24a abut on each other, so that a portion of the amorphous silicon layer 22 between the first blocking pattern 23-1 and the
5 second blocking pattern 23-2 is covered.

Referring now to FIGs. 2D and 3D, a first metal layer 25 is formed over the entire surface of the substrate 20. The first metal layer 25 directly contacts the exposed end portions of the amorphous silicon layer 22. The first metal layer 25 preferably has a thickness of hundreds of Å and is preferably made of a material which can react with silicon (Si) to form a silicide such as
10 Ni or Pd.

Referring now to FIGs. 2E and 3E, the first and second reflowed photoresist patterns 24-1a and 24-2a are removed to expose the blocking layer 23 and to expose an offset region “dos” of the amorphous silicon layer 22. Therefore, the first metal layer 25 remains only on both end portions of the amorphous silicon layer 22.

15 Referring now to FIGs. 2F and 3F, the amorphous silicon layer 22 is crystallized at a temperature of preferably 400 °C to 600 °C to form a poly silicon layer 22. At this moment, both end portions of the amorphous silicon layer 22 that directly contact the metal layer 25 are crystallized by the MIC, and a non-contact portion of the amorphous silicon layer 22 that does not contact the metal layer 25 is crystallized by the MILC. The poly silicon layer 22 includes
20 poly silicon layers 22a and 22b. The poly silicon layer 22a includes first and second poly silicon layers 22-1 and 22-2, and the poly silicon layer 22b includes first and second poly silicon layers 22-3 and 22-4. The first poly silicon layers 22-1 and 22-3 are formed by the MILC, and the second poly silicon layers 22-2 and 22-4 are formed by the MIC. Also, an MILC front 22-5

exists between the poly silicon layers 22a and 22b. The first metal layer 25 remaining on the poly silicon layers 22a and 22b is removed to expose the second poly silicon layers 22-2 and 22-4.

Referring now to FIGs. 2G and 3G, using the first blocking pattern 23-1 and the second blocking pattern 23-2 as a mask, the poly silicon layers 22a and 22b are etched to form first and second semiconductor layers 30a and 30b (see FIGs. 2H and 3H). Therefore, the first and second semiconductor layers 30a and 30b include only the MILC regions 22-2 and 22-4, respectively. The MILC front 22-5 is removed while etching the poly silicon layers 22a and 22b. Thereafter, the blocking layer 23 is removed.

Referring now to FIGs. 2H and 3H, a surface treatment process is performed in order to improve a surface characteristic of the semiconductor layers 30a and 30b. The surface treatment process is to remove a natural oxide layer (not shown) or impurities on the semiconductor layers 30a and 30b and is performed using a dry-etching technique or an HF etching solution of 0.1 % to 20 %.

At this point, in case the blocking layer 23 is made of an oxide layer, the surface treatment process can be performed at the same time as the process of removing the blocking layer 23.

Referring now to FIGs. 2I and 3I, the TFT having a dual channel is completed using the first and second semiconductor layers 30a and 30b. In greater detail, a gate insulating layer 26 is formed over the entire surface of the substrate 20. A second metal layer is deposited over the entire surface of the substrate 20 and patterned to form a gate line 27a and a gate electrode 27b. The gate electrode 27b extends from the gate line 27a.

Subsequently, using the gate electrode 27b as a mask, a p- or an n-type high-density

impurity is ion-implanted into the first and second semiconductor layers 30a and 30b to form first source and drain regions 29a and 29b and second source and drain regions 29c and 29d, respectively. The non-doped portions of the first and second semiconductor layers 30a and 30b serve as a channel area.

5 At this point, an offset region or a lightly doped drain (LDD) region can be formed between the source and drain regions and the channel area. The method of forming the offset region or the LDD region is well known.

Next, an interlayer insulating layer 31 is formed over the entire surface of the substrate 20. The interlayer insulating layer 31 includes contact holes 31a to 31d. The contact holes 31a and 31b are formed at a location corresponding to a portion of the first source region 29a and to a
10 and 31b are formed at a location corresponding to a portion of the first source region 29a and to a portion of the first drain region 29b, respectively. The contact holes 31c and 31d are formed at a location corresponding to a portion of the second source region 29c and to a portion of the second drain region 29d, respectively.

Thereafter, a third metal layer is deposited on the interlayer insulating layer 31 and
15 patterned to form source and drain electrodes 32a and 32b and a data line 32c. The source electrode 32a extends from the data line 32c and is electrically connected to the first and second source regions 29a and 29c, respectively, through the contact holes 31a and 31c. The drain electrode 32b is electrically connected to the first and second drain regions 29b and 29d, respectively, through the contact holes 31b and 31d. Consequently, the TFT according to the
20 present invention is completed.

As described herein, the TFT according to an embodiment of the present invention has numerous advantages. Since a mask process to crystallize the amorphous silicon layer is not required, the manufacturing process is simplified, thus leading to a high manufacturing yield.

Also, since the MILC front is removed, the formation of defects can be prevented, leading to high reliability.

Referring now to FIGs. 4A and 5A, a buffer layer 41 and an amorphous silicon layer 42 are sequentially formed on an insulating substrate 40. The buffer layer 41 is preferably made of an oxide layer and serves to prevent an impurity from being diffused into a semiconductor layer which will be formed in subsequent process. At this point, the buffer layer 41 and the amorphous silicon layer 42 can be formed using the PECVD technique. Thereafter, a photoresist pattern 43 is formed on the amorphous silicon layer 42 while exposing both end portions of the amorphous silicon layer 42.

Referring now to FIGs. 4B and 5B, a first metal layer 44 is formed over the whole surface of the substrate 40 and covers the photoresist pattern 43. The first metal layer 44 is preferably made of a material which reacts with silicon to form a silicide such as Pd or Ni. The first metal layer 44 preferably has a thickness of 1 Å to 5000 Å and preferably tens to hundreds of Å and directly contacts the exposed end portions of the amorphous silicon layer 42.

Referring now to FIGs. 4C and 5C, the photoresist pattern 43 is removed to expose a central portion of the amorphous silicon layer 42. The first metal layer 44 remains only on both end portions of the amorphous silicon layer 42.

Referring now to FIGs. 4D and 5D, the amorphous silicon layer 42 is crystallized at a temperature of preferably 400 °C to 600 °C to form a poly silicon layer 42a. The exposed portion of the amorphous silicon layer 42 is crystallized by the MILC, and both end portions of the amorphous silicon layer 42 which directly contact the first metal layer 44 are crystallized by the MIC.

At this juncture, since a contact region between the amorphous silicon layer 42 and the

first metal layer 44 is relatively large, a crystallization speed will increase. An MILC front 42-3 exists on a central portion of the poly silicon layer 42a (*i.e.*, MILC region 42-1).

Referring now to FIGs. 4E and 5E, the first metal layer 44 remaining on MIC regions 42-2 of the poly silicon layer 42a is removed.

5 Referring now to FIGs. 4F and 5F, a photoresist pattern 45 is formed on the poly silicon layer 42a. The photo resist pattern 45 includes first and second photoresist patterns 45-1 and 45-2. The first and second photoresist patterns 45-1 and 45-2 are formed on the corresponding MILC regions 42-1, respectively, and are spaced apart from each other, so that the MILC front 42-3 is exposed.

10 Referring now to FIGs. 4G and 5G, using the photoresist pattern 45 as a mask, the poly silicon layer 42 is etched to form first and second semiconductor layers 43a and 43b. At the same time, the MILC front 42-3 is removed. Therefore, the first and second semiconductor layers 43a and 43b include only the MILC regions 42-1. Thereafter, the photoresist pattern 45 is removed.

Subsequently, a surface treatment process is performed in order to improve a surface
15 characteristic of the semiconductor layers 43a and 43b. The surface treatment process is to remove a natural oxide layer (not shown) or impurities on the semiconductor layers 43a and 43b and is performed using a dry-etching technique or an HF etching solution of 0.1 % to 20 %.

Thereafter, even though not shown in the drawings, the process of FIGs. 2I and 3I is performed to complete the TFT according to another embodiment of the present invention.

20 As described herein, the TFT according to an embodiment of the present invention has numerous advantages. First, since crystallization simultaneously processes from all edge portions of the amorphous silicon layer, the processing time is reduced. Second, since the MILC front is removed, the formation of defects is prevented, thereby improving reliability. Third,

traps are prevented since the boundaries between the MIC and MILC regions are located outside the channel area, *for example*, within the source and drain regions, thereby improving electric field mobility. Fourth, since the amorphous silicon layer is crystallized without an additional mask process, the manufacturing process is simplified, leading to a high manufacturing yield.

- 5 While the invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in form and details may be made therein without departing from the spirit and scope of the invention.